Customer No.: 31561
Application No.: 10/709,090
Docket No.:12029-US-PA

## AMENDMENT

**To the Claims:**

Claim 1. (currently amended) A pixel structure, comprising:

a scan line, disposed over a substrate;

a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;

a plurality of transparent capacitance electrodes, disposed over the substrate, wherein the transparent capacitance electrodes comprises at least a first transparent capacitance electrode and at least a second transparent capacitance electrode disposed above the first transparent capacitance electrode; and

a pixel electrode, ~~disposed over the transparent capacitance electrodes and electrically connected to the active component, wherein the pixel electrode and the transparent capacitance electrodes constitute a multilayer pixel storage capacitor~~ electrically connected to the first transparent capacitance electrode and the active component, wherein at least a first pixel storage capacitor is formed between the first transparent capacitance electrode and the second transparent capacitance electrode, and at least a second pixel storage capacitor parallel connected to the first pixel storage capacitor is formed between the second transparent capacitance electrode and the pixel electrode.

Claim 2. (original) The pixel structure of claim 1, wherein a portion of the transparent capacitance electrode is electrically connected to the active component.

Claim 3. (original) The pixel structure of claim 1, wherein a portion of the transparent capacitance electrode is electrically connected to the pixel electrode, and electrically connected to the active component via the pixel electrode.

Claim 4. (original) The pixel structure of claim 1, wherein the active component comprises a low temperature polysilicon (LTPS) thin film transistor (TFT).

Claim 5. (original) The pixel structure of claim 4, further comprising:

a source/drain conductive layer, wherein the active component is electrically connected to the data line and the pixel electrode via the source/drain conductive layer.

Claim 6. (original) The pixel structure of claim 4, further comprising:

a conductive layer, wherein the active component is electrically connected to the data line via the conductive layer, and the pixel electrode is electrically connected to the active component.

Claim 7. (original) The pixel structure of claim 1, wherein the active component comprises an amorphous silicon (a-Si) thin film transistor (TFT).

Claim 8. (original) The pixel structure of claim 7, wherein the active component comprises:

a gate, electrically connected to the scan line;

a channel, disposed over the gate; and

a source/drain, disposed over the channel and electrically connected to the data line and the pixel electrode.

Claim 9. (original) The pixel structure of claim 1, wherein a material of the pixel electrode and the transparent capacitance electrode comprise an indium tin oxide (ITO) or an indium zinc oxide (IZO).

Claim 10. (currently amended) A manufacturing method, for a pixel structure, comprising:

sequentially forming an active component, a scan line and a data line over a substrate, wherein the active component is electrically connected to the scan line and the data line;

forming a plurality of transparent capacitance electrodes over the substrate, wherein the transparent capacitance electrodes comprises at least a first transparent capacitance electrode and at least a second transparent capacitance electrode formed above the first transparent capacitance electrode; and

forming a pixel electrode over the transparent capacitance electrodes, wherein the pixel electrode is electrically connected to the active component, wherein ~~the pixel electrode and the transparent capacitance electrodes constitute a multilayer pixel storage capacitor~~ at least a first pixel storage capacitor is formed between the first transparent capacitance electrode and the second transparent capacitance electrode, and at least a

second pixel storage capacitor parallel connected to the first pixel storage capacitor is formed between the second transparent capacitance electrode and the pixel electrode.

Claim 11. (original) The manufacturing method of claim 10, wherein the active component comprises a low temperature polysilicon (LTPS) thin film transistor (TFT).

Claim 12. (original) The manufacturing method of claim 11, wherein a source/drain conductive layer over the active component during the step of forming the data line, wherein the active component is electrically connected to the data line and the pixel electrode via the source/drain conductive layer.

Claim 13. (original) The manufacturing method of claim 11, further comprises a step of forming a conductive layer over the active component after the step of forming the data line, wherein the active component is electrically connected to the data line via the conductive layer, and the pixel electrode is electrically connected to the active component.

Claim 14. (original) The manufacturing method of claim 13, wherein the conductive layer and the pixel electrode is formed by patterning a same material layer.

Claim 15. (original) The manufacturing method of claim 11, wherein the step of forming the active component comprises:

forming a polysilicon layer over the substrate;

forming an inter-gate dielectric layer over the substrate covering the polysilicon layer;

forming a gate over the inter-gate dielectric layer and the polysilicon layer; and

forming a doped source/drain region in the polysilicon layer on both sides of the gate.

Claim 16. (original) The manufacturing method of claim 15, wherein the step of forming the doped source/drain region comprises:

performing an ion implantation process using the gate as a mask to form the doped source/drain region on both sides of the polysilicon layer.

Claim 17. (original) The manufacturing method of claim 10, wherein the active component comprises an amorphous silicon (a-Si) thin film transistor (TFT).

Claim 18. (original) The manufacturing method of claim 17, wherein the step of forming the active component comprises:

forming a gate over the substrate, wherein the gate is electrically connected to the scan line;

forming an inter-gate dielectric layer over the substrate covering the gate;

forming a channel over the inter-gate dielectric layer, wherein the channel is disposed over the gate; and

forming a source/drain over the channel.

Claim 19. (original) The manufacturing method of claim 10, wherein a material of the pixel electrode and the transparent capacitance electrodes comprise an indium tin oxide (ITO) or an indium zinc oxide (IZO).

Claim 20. (previously presented) A pixel structure, comprising:

a scan line, disposed over a substrate;

a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;

a first transparent capacitance electrode, disposed over the substrate;

a pixel electrode, disposed over the first transparent capacitance electrode and electrically connected to the active component and the first transparent capacitance electrode; and

a second transparent capacitance electrode, disposed between the first transparent capacitance electrode and the pixel electrode, wherein a multilayer pixel storage capacitor is formed by the pixel electrode, the first transparent capacitance electrode and the second transparent capacitance electrode.

Claim 21. (previously presented) The pixel structure of claim 20, wherein the second transparent capacitance electrode is electrically insulating from the first transparent capacitance electrode and the pixel electrode.

Claim 22. (currently amended) A pixel structure, comprising:

a scan line, disposed over a substrate;

a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component comprises a gate electrically connected to the scan line, a channel disposed over the gate and a source/drain disposed over the channel and electrically connected to the data line and the pixel electrode;

a protection layer, disposed over the substrate for covering the gate of the active component;

a plurality of transparent capacitance electrodes, disposed over the substrate, the transparent capacitance electrodes comprising at least a first transparent capacitance electrode and at least a second transparent capacitance electrode disposed above the first transparent capacitance electrode, wherein the first transparent capacitance electrode is disposed on the protection layer; and

a pixel electrode, ~~disposed over the transparent capacitance electrodes and electrically connected to the active component, wherein the pixel electrode is electrically connected to the first transparent capacitance electrode such that the transparent capacitance electrodes constitute a multilayer pixel storage capacitor~~ electrically connected to the first transparent capacitance electrode and the active component, wherein at least a first pixel storage capacitor is formed between the first transparent capacitance electrode and the second transparent capacitance electrode, and at least a second pixel storage capacitor parallel connected to the first pixel storage capacitor is formed between the second transparent capacitance electrode and the pixel electrode.